REMARKS

Applicant has amended claims 1, 5, 6, 9, 18 to 30, and 32, added claims 33 and 34, and canceled claim 15.

Claim Objection

The Examiner objected to claims 19 to 27 for reciting a "controller node" instead of a "node controller." The Examiner further objected to claim 32 for reciting the "data storage devices" instead of the "data storage device." Applicant has amended claims 19 to 27 and 32 to correct these informalities.

§ 102 Rejections

U.S. Patent No. 6,026,464 ("Cohen")

The Examiner rejected claims 1, 3 to 16, 28 to 30, and 32 under 35 U.S.C. § 102(b) as being anticipated by Cohen.

Addressing claim 1, the Examiner stated:

> Cohen discloses a node controller (Figure 1, 18) for a node in a data storage system having at least two nodes (Node 1:CPU 14 and Memory Controller 18A, Node 2: CPU 16 and Memory Controller 18; Node 3: Memory Controller 18, Network Controller 26, Storage Controller 28, etc., Node 4: Memory Controller 18, Display Controller, etc.) the node controller being distinct from a computer-memory complex of the node (Column 3, Lines 10-12; CPU has a cache and therefore is a computer-memory complex, i.e. processing system), the node controller being operable to transfer data between the two nodes as instructed by the computer-memory complex but without any further intervention by the computer-memory complex (Column 3, Lines 22-25 and 48-49).

12/23/04 Office Action, p. 2, paragraph 6.

The Examiner identified four "nodes" in global memory system 12 of Cohen. Applicant has amended claim 1 to distinguish the nodes in the data storage system recited in claim 1 from the "nodes" in global memory system 12 of Cohen identified by the Examiner. Specifically, each node is amended to include one computer-memory complex and one node controller distinct from the computer-memory complex. Amended claim 1 now recites:

> 1. A node controller for a node in a data storage system having at least two nodes, each node comprising one computer-memory complex and one node controller distinct from said one computer-memory complex, the node controller being operable to transfer data between the two nodes as instructed by a computer-memory complex of the node but without any further intervention by the computer-memory complex, the node controller comprising a cluster memory for storing the data being transferred between the two nodes.

Amended claim 1 (emphasis added). By amending claim 1, Applicant has removed "Node 3" and "Node 4" of Cohen as the nodes recited in claim 1 because they do not have a computer-memory complex as recited in claim 1.

The Examiner identified CPU 14 and memory controller 18A as "Node 1," and CPU 16 and memory controller 18 as "Node 2." However, neither "Node 1" nor "Node 2" includes a "node controller being operable to transfer data between the two nodes" as recited in claim 1.

> The memory controller 18 receives access requests from the connected processing device(s), and then checks the state of the addressed memory bank 70. For example, memory controller 18A reviews requests from CPU 14. If that targeted memory bank 70 is idle, the memory controller 18 arbitrates for the memory bus 22 and "activates" that memory bank 70. Each memory controller 18 sees the activate command and marks that memory bank 70 as busy. When the data for the activated memory bank 70 is ready for access, the memory controller 18 arbitrates a second time for a data bus transaction. When granted the data bus, the memory controller 18 bursts the data from the memory subsystem 20 for a read or writes the data into the memory subsystem 20. When the data bus transaction is completed, each memory controller 18 marks that memory bank 70 idle.

Cohen, col. 3, lines 48 to 62 (emphasis added). Cohen only discloses that memory controllers 18 and 18A write to and read from memory subsystem 20 in global memory system 12. Cohen does not disclose that memory controllers 18 and 18A "being operable to transfer data between the two nodes" as recited in claim 1.

Claim 1 is further patentable over Cohen for reciting a cluster memory in a node controller that is distinct from a system memory understood to be in a computer-memory complex. Fig. 2 of the present disclosure illustrates a computer-memory complex 18 in one embodiment of the invention. As can be seen, computer-memory complex 18 includes one or more CPUs 30a and 30b connected by a main controller 24 to a system memory 32. On the other hand, Cohen shows a single memory subsystem 20 shared by all the components in a global memory system 12. Accordingly, claim 1 is patentable over Cohen because its memory subsystem 20 cannot be both the cluster memory in the node controller and the system memory in the computer-memory complex.

Claims 3 to 8 and 28 depend from claim 1 and are patentable over Cohen for at least the same reasons as claim 1.

The Examiner rejected claim 9 by asserting that "[i]t is inherent the address comparator performs logic operations on the address data." 12/23/04 Office Action, ¶ 14. Applicant has amended claim 9 as follows:

> 9. A node controller for a node in a data storage system having at least two nodes, each node comprising one computer-memory complex and one node controller distinct from said one computer-memory complex, the node controller comprising:
>
> a plurality of logic engines each operable to perform a logic operation on storage data originating from at least one data source in the data storage system and to write a result of the logic operation to at lease one data destination in the data storage system, the logic engine performing the logic operation as instructed by a computer-memory complex of the node but without any further intervention by the computer-memory complex; and
>
> command queues coupled to the logic engines, the command queues operable to store logic control blocks which can be processed by the logic engines.

Claim 9 (emphasis added). As used herein, the "storage data" differentiate the actual data from any address or command that may accompany the actual data. While Cohen discloses that a comparison operation is performed on the address, it does not disclose that a logic operation is performed on storage data and the result of the logic operation is written to a data destination in the data storage system. Thus, claim 9 is patentable over Cohen.

Claims 10 to 14 and 16 depend from claim 9 and are patentable over Cohen for at least the same reasons as claim 9. Applicant has canceled claim 15, thereby rendering its rejection moot.

The Examiner rejected claim 29, 30, and 32. Addressing claim 29, the Examiner asserted that Cohen discloses "the node controller being distinct from a computer-memory complex of the first node (Column 3, Lines 10-12; CPU has a cache and therefore is a computer-memory complex, i.e. processing system)." 12/23/04 Office Action, p. 5, ¶ 22. Applicant respectfully traverses.

As discussed above in regards to claim 1, the computer-memory complex includes one or more CPUs 30a and 30b connected by a main controller 24 to a system memory 32. Using the Examiner's argument, CPUs 30a and 30b would also have cache memories built into the processors

in addition to system memory 32. Thus, Cohen still does not show a corresponding system memory because the Examiner already identified Cohen's memory subsystem 20 as the recited "cluster memory" of claim 29. Accordingly, claim 29 is patentable over Cohen because its memory subsystem 20 cannot be both the cluster memory in the node controller and the system memory in the computer-memory complex.

Claims 30 and 32 depend from claim 29 and are patentable over Cohen for at least the same reasons as claim 29.

U.S. Patent No. 5,842,038 ("Williams et al.")

The Examiner rejected claims 1, 9, 18, and 29 under 35 U.S.C. 102(b) as being anticipated by Williams et al. Williams et al. discloses a system 10 for separating read and write commands to a memory. See Fig. 1. Specifically, an uplink 100 includes a command decoder 110 that directs the read commands to a read buffer 106 and the write commands to a write buffer 108. Williams et al., col. 5, lines 18 to 24. Command decoder 110 separates the read and write commands according to a command field 158 in a command structure 150. Williams et al. col., lines 39 to 61. The write command would include both the command and the data to be written. Williams et al., col. 6, lines 17 and 18.

Amended claim 1 now recites "each node comprising one computer-memory complex and one node controller distinct from said one computer-memory complex" and "the node controller comprising a cluster memory for storing data being transferred through the node." Claim 1. Main memory storage units 22 to 24 of Williams et al. cannot be both the cluster memory in the node controller and the system memory in the computer-memory complex. Accordingly, claim 1 is patentable over Williams et al.

Amended claim 9 now recites that "a plurality of logic engines each operable to perform a logic operation on storage data originating from at least one data source in the data storage system and to write a result of the logic operation to a data destination in the data storage system." Claim 9. While Williams et al. discloses that a comparison operation is performed on command field 158, it does not disclose that a logic operation is performed on storage data and the result of the logic operation is written to a data destination in the data storage system. Accordingly, claim 9 is patentable over Williams et al.

Amended claims 18 and 29 recite similar language as amended claims 1 and 9. Thus, claims 18 and 29 are patentable over Williams et al. for at least the same reasons as claims 1 and 9.

§ 103 Rejections

The Examiner rejected claims 18 to 27 and 31 under 35 U.S.C. § 103(a) as being unpatentable over Cohen in view of U.S. Patent No. 5,959,860 ("Styczinski"). Applicant respectfully traverses.

Addressing claim 18, the Examiner cited Cohen for disclosing a logic engine for performing logic operation on data, and Styczinski for disclosing a logic engine for performing logic operation to one of a plurality of data sources and writing the result to one of a plurality of data destinations. Applicant assumes the Examiner found it to be obvious to modify the identified logic engine in Cohen with the teachings of Styczinski. However, the logic engine identified by the Examiner in Cohen is an address comparator that operates on address data. One skilled in the art would not be motivated to modify an address comparator to operate on storage data. Furthermore, neither Cohen nor Styczinski discloses a node controller with a cluster memory that is distinct from a computer-memory complex with a system memory. Accordingly, claim 18 is patentable over any combination of Cohen and Styczinski.

Claims 19 to 27 depend from claim 18 and are patentable over the cited references for at least the same reasons as claim 18.

Claim 31 depend from claim 29 and is patentable over the cited references for at least the same reasons as claim 29.

New claims

New claim 33 depends from claim 9 and is patentable over the cited references for at least the same reasons as claim 9.

New claim 34 depends from claim 28 and is patentable over the cited references for at least the same reasons as claim 28.

In summary, claims 1, 3 to 16, 17 to 32 were pending in the above-identified application when last examined. This Amendment amends claims 1, 5, 9, 18 to 30, and 32, adds claims 33 and 34, and

cancels claim 15. For the above reasons, Applicant respectfully requests the Examiner with withdraw the claim rejections and allow claims 1, 3 to 14, 16, 18 to 34. Should the Examiner have any questions, please call the undersigned at (408) 382-0480x206.

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